What is claimed is:

1. A field effect transistor (FET) device comprising a surface of the channel region being corrugated.

2. The field effect transistor (FET) device of claim 1 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

3. The field effect transistor (FET) device of claim 1 wherein the at least one of:

the surface of the channel region, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

4. The field effect transistor (FET) device of claim 1 wherein only the interface of the channel region covered by the gate electrode is corrugated.

5. The field effect transistor (FET) device of claim 1 wherein only the upper surface of the gate electrode is corrugated.

6. The field effect transistor (FET) device of claim 1 wherein both the interface of the channel region covered by the gate electrode and the upper surface of the gate electrode are corrugated.

7. The field effect transistor (FET) device of claim 1 wherein the gate electrode is formed to a thickness of from about 500 to about 2000 angstroms.

8. A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate and covering a channel region within the semiconductor substrate a gate electrode; and

forming within the semiconductor substrate and separated by the channel region within the semiconductor substrate a pair of source/drain regions, wherein at least one of:

an interface of the channel region covered by the gate electrode; and

an surface of the channel region, is corrugated.

9. The method of claim 8 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

10. The method of claim 8 wherein the at least one of:

the interface of the channel region covered by the gate electrode; and

the upper surface of the gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.04 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

11. The method of claim 8 wherein only the interface of the channel region covered by the gate electrode is corrugated.

12. The method of claim 8 wherein only the upper surface of the gate electrode is corrugated.

13. The method of claim 8 wherein both the interface of the channel region covered by the gate electrode and the upper surface of the gate electrode are corrugated.

14. The method of claim 8 wherein the gate electrode is formed to a thickness of from about 600 to about 200 angstroms.